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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Cynthia Bertini, et al.

Serial No.:	10/065,801	Group Art Unit:	2128
Filed:	11/20/2002	Examiner:	Patel, Shambhavi K.
For:	METHOD AND SYSTEM FOR MANAGING ELECTRICAL SCHEMATIC DATA		
Atty Docket No:	81045450		

I hereby certify that this correspondence is being transmitted via facsimile (571-273-8300) to Examiner Shambhavi K. Patel with the United States Patent and Trademark Office on:

August 18, 2006 **Jo Anne Croskey**
Date of Deposit

Jo Anne Croskey
Signature

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner:

The Applicants, respectfully, request a Pre-Appeal Brief Request for Review in view of improper rejections based upon error(s) in fact and based upon essential element(s) required to establish a *prima facie* rejection. This Request is submitted along with a Notice of Appeal.

In the Advisory Action dated August 10, 2006, claims 1-24 are pending. Claims 1, 11, and 19 are independent claims from which all other claims depend therefrom.

The Advisory Action states that the amendments are deemed not to place the application in a better form for appeal. Applicants submit that there are and have not been any claim amendments submitted.

The Advisory Action further states that Applicants' arguments are not persuasive in view of Examiner's response to the remarks submitted on March 6th, 2006. The Examiner maintains that the prior art reference to Heile discloses a logical schematic, a layout schematic, and a physical schematic. This is the only argument provided in the Advisory Action. The Advisory Action does not address the valid arguments that were provided by the Applicants in the Response of July 20, 2006, including that which was provided with regards to the Van Huben and Tou references. The arguments provided in the July 20th Response are valid, maintained, and are reiterated below along with additional arguments for the allowability of the recited claims.

First addressing the Advisory Action argument, that Heile discloses the stated schematics, Applicants submit that Heile clearly fails to disclose the schematics claimed. See below arguments. Applicants believe that Heile discloses a high level block diagram, a logical schematic, and an overall design or logic device layout, which includes logic device groupings. As such, Heile only discloses one schematic. Nevertheless, regardless of how many schematics or the types of schematics that the Examiner feels that Heile discloses, Heile undoubtedly fails to disclose all of the schematics claimed, as defined by the specification of the present application. Heile further fails to disclose the formation of a part master file containing the claimed schematics.

Claims 1, 3-6, 8-12, 14-19, and 21-24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Heile (6,289,315). Applicants, respectfully, traverse.

Claim 1 is directed to a method for managing electrical schematic data comprising creating a logical schematic, a layout schematic, and a physical schematic for a part. Claim 1 further recites associating the logical schematic, the layout

schematic, and the physical schematic together to form a part master file. The part master file is stored on a computer network. Claim 1 further recites providing access to the part master file to multiple user locations and controlling modification of the part master file so that only one of the user locations is allowed to modify the part master file at a time.

In paragraph [0017] of the specification of the present application, the Applicants have specifically and explicitly defined what is meant and referred to by the terms "logical schematic", "layout schematic", and "physical schematic." The term "logical schematic" is defined as a schematic diagram comprising the logical layout of the electrical system that it describes. The logical layout is one that fully describes the electrical relationship of the circuit, but does not necessarily describe the electrical components used or the physical positioning of those components. The term "layout schematic" is defined as a schematic diagram that shows the electrical components used in the design and the connections between them, i.e., the layout, but does not describe the exact physical positioning of the components. The "physical schematic" is defined as a schematic diagram that fully describes the electrical components used and their connections, showing the exact physical positioning of the components.

Applicants understand that limitations from the specification ought not to be read into the claims. Applicants also understand that, in general, claim terms ought to be given their broadest reasonable interpretation. However, Applicants are also aware that they are entitled to be their own lexicographer. See *In re Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994). Applicants are further aware that when ever an explicit definition is provided by the Applicants for a term, that definition will control the interpretation of the term as it is used in the claim. See *Intellical, Inc. v. Phonometrics, Inc.*, 952 F.2d 1384, 1387-88, 21 USPQ2d 1383, 1386 (Fed. Cir. 1992). As such, the above definitions ought to be used when interpreting the claims of the present application.

The Office Action states that Heile discloses a logical schematic, a layout schematic, and a physical schematic. Applicants traverse and submit that Heile may

disclose a logical schematic, but clearly fails to show, teach, or suggest a layout schematic and a physical schematic as defined and claimed by the present application. Heile discloses the use of a high level block diagram of a design methodology that is used to develop a design for a programmable logic device (PLD). The blocks in the block diagram are non-implemented or un-finished and are used to create templates, which are starting points for the actual design. The high level block diagram, in other words, is used prior to the creation of a logical schematic of the electrical system or the PLD. Upon creation of the templates, the system of Heile takes the source or root file of the high level block diagram and performs a simulation. In the simulation, a block functionality is reviewed by a designer. Once the results of the simulation are satisfactory the entire design or block diagram is simulated, in which case the entire block diagram is compiled. In compilation, the language for the blocks is converted to perform a simulation. The final layout or overall design, an example of which is shown and described with respect to Figure 18 of Heile, has the gates or logic devices and the layout thereof that represent the logic of that design. The logic devices are not the actual electrical hardware components, but rather represent the logic for the hardware components.

Throughout Heile the generation of the overall design is described. Although in col. 22, lines 42-46, Heile discloses that the overall design may be mapped, such that the logic gates are grouped. Each group corresponds to a physical device that is to perform the functions of that group. The groupings are merely hyphened blockings of the logic gates. The groupings do not show the electrical components used in the design and the connections between them or the exact physical positioning of those components, as required by the above definitions of the claimed terms. Thus, Heile only discloses a logical schematic.

The Office Action states that Heile discloses a layout schematic in col. 7, lines 49-52. In col. 7, lines 49-52, Heile discloses the compilation of the high level block diagram for the entire original design for simulation purposes. Heile does not disclose any

electrical components used in the design and the connections between them. The layout referred to in lines 49-52 is merely the high-level block diagram layout, which is unlike that claimed.

The Office Action further states that Heile discloses a physical schematic in col. 7, lines 34-35 and 52-57. In the stated sections, Heile discloses the design connectivity of the high level block diagram and again the compilation of that block diagram. No physical schematic is disclosed.

The Office Action then states that the schematics of Heile are also referred to as design files, source files, or programming files. Applicants submit that regardless of whether this is true, it is irrelevant. Applicants submit that however or whatever the high level block diagram and the finalized logical layout or design of Heile is referred to as, the stated diagram and design are not the same as the layout schematic and physical schematic claimed, as clearly shown above. Thus, regardless of whether Heile links the high level block diagram and finalized logical layout or design into a master file or project file, Heile fails to teach or suggest to of the three schematics claimed and the linking thereof.

The Office Action states that the teaching in Heile is directed to the compilation process for a traditional integrated circuit design and does not address the association or lack thereof between any of the logical, layout, or physical schematics. Applicants admit that Heile is directed to the compilation process of a traditional integrated circuit design. However, the stated process only provides a logical schematic or design. The layout and physical schematics that may be associated with that design are not addressed in Heile because they are not part of the compilation process. Heile does not disclose or speak to layout and physical schematics and as such fails to teach or suggest a majority of the claimed limitations.

As such, the Applicants maintain the Heile reference fails to teach or suggest the formation of a part master file from a logical schematic, a layout schematic, and a physical schematic as recited in the independent claims 1, 11, and 19. Applicants also

maintain that since claims 3-6, 8-10, 12, 14-18, and 21-24 depend from their respective independent claims, that they are also believed to be allowable for at least the same reasons as set forth above.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Heile in view of Van Huben (6,094,654). Applicants traverse.

The Office Action further argues that Van Huben discloses a pointer that indicates a storage location of data. Applicants have admitted that a pointer is set forth in the Van Huben reference. However, the Applicants maintain that the Van Huben reference does not teach or suggest the further step of storing a pointer in a part master file wherein the pointer indicates a storage location of a logical schematic, a physical schematic, and a layout schematic. In fact, like the Heile reference, there is no teaching or suggestion in the Van Huben reference for associating the three types of schematics, logical, layout, and physical together in one file. The Office Action is silent with respect to this argument.

Applicants therefore respectfully request the Examiner to reconsider the rejection of Claim 7 as well.

Claims 3, 13 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Heile in view of Tou (Knowledge-Based Approach for the Verification of CAD Database Generated by an Automatic Schematic Capture System). Applicants traverse.

Applicants submit that since claim 3 depends from claim 1,that it too is novel, nonobvious, and is in a condition for allowance for at least the same reasons.

With respect to claims 13 and 20, Applicants have agreed with the Examiner that Heile fails to teach using a logical schematic, a layout schematic, and a physical schematic to form a schematic image file.

Also, with respect to claims 13 and 20, the Examiner states that the Applicants argued that the Tou reference does not teach using design files to create a schematic image file. Applicants submit that this is not what Applicants argued in the Response of March 6, 2006, although Applicants do believe this to be a true statement. Applicants

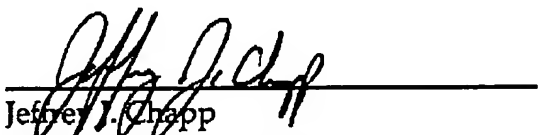
argued that the Tou reference does not teach the creating of a part master file from a logical schematic, layout schematic and physical schematic. This is clearly the case, since Tou is not directed to the creation of a part master file having multiple schematics. As admitted in the Office Actions Tou is directed to the interpretation of circuit diagrams from their images. Tou discloses the interpreting or processing of schematic image files into machine readable data files of which a CAD software can read. Simply put, Tou teaches converting an image file into a readable CAD file. This is unlike that recited in claims 13 and 20, which recite the inclusion of a schematic image file based on a logical schematic, a layout schematic, and a physical schematic. The conversion or translation of one file into another file is not the same as the generation of a file based on three other files. Also, the conversion of an image file into a data file is different that the generation of an image file based on three schematic files. Furthermore, claims 13 and 20 do not recite any conversion of schematics, but rather recite the formation of an image file based on schematics.

Applicants further note that the disclosure of a CAD system, software, or files does not suggest the formation of an image file as claimed. Tou discloses the conversion of image files into CAD readable data, such that they can be used for further design. Again the conversion of a file into a CAD format does not speak to the generation of an image file based on the schematics claimed. Thus, Tou does not disclose the generation of a schematic image file as claimed and to assert otherwise would be inconsistent with the Tou reference and the present application.

Therefore, Applicants respectfully request the panel to reverse the Examiner's position with respect to each and every one of the pending claims based upon the errors in fact and the essential elements missing to establish a *prima facie* case. The application is in condition for allowance and expeditious notice thereof is earnestly solicited. Should the Panel Examiners have any questions or comments, they are respectfully requested to contact the undersigned attorney.

The Commissioner is hereby authorized to charge any additional fees, which may be required, or credit any overpayment to Deposit Account No. 06-1510.

Respectfully submitted,



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Date: August 18, 2006

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